IDEC Chip Design Contest

Low-power 20 pJ/conversion-step 12-bit SAR resistance-to-digital converter for microsensors

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ABSTRACT

In this paper, a low-power 12-bit successive approximation register (SAR) resistance-to-digital converter (RDC) for resistive microsensors with a figure-of-merit (FoM) of 20 pJ/conversion-step is presented. In the conventional resistive analog front-end (AFE), two-step conversion schemes, including a resistance-to-voltage converter and a voltage-to-digital converter are generally used. The presented SAR RDC can directly convert the resistance changes to digital codes. The proposed SAR RDC consists of a comparing stage, and a SAR operating stage. The preamplifier of comparing stage implements a correlated double sampling (CDS) technique to improve the low-noise characteristic and reduce the low-frequency flicker (1/f) noise. The RDC is designed using SAR scheme to achieve low-power consumption. The SAR RDC achieves a wide input resistance range of 2 MΩ. The SAR RDC is implemented with a 0.18 µm standard complementary metal–oxide–semiconductor (CMOS) process. All functional blocks, including voltage and current references, oscillators, and timing generators, are integrated on the chip. The proposed RDC consumes 90 µW with 1.8 V power supply. The simulated SAR RDC achieve 12-bit resolution within a conversion time of 0.92 ms and a figure-of-merit (FoM) of 20 pJ/conversion-step.

INTRODUCTION

- In recent years, various resistive sensor interface integrated circuits (IC) have been developed. The resistive sensor interface circuit converts the resistance into a digital signal for the back-end digital signal processing (DSP)A chopper-stabilization technique is adopted to reduce the 1/f noise and DC offset.
- In previous research studies, resistive sensor interface circuit with a delta-sigma analog-to-digital converter (ADC) was proposed. However, delta-sigma ADCs suffers from high power consumption of the modulator and requires additional digital filtering. Due to base on a sequencer and a register, the successive approximation register (SAR) scheme is one of the low-power consumption technique.
- The proposed SAR resistance-to-digital converter (RDC) consists of a comparing stage, and a SAR operating stage. The preamplifier was used at the comparing stage for faster and more accurate comparisons.
- In the preamplifier of the proposed resistive sensor interface IC, a correlated double sampling (CDS) technique was applied to remove the low-frequency flickering (1/f) noise and DC offset in the amplifier.

CIRCUIT IMPLEMENTATION

- Proposed SAR RDC
  - Fig. 1 shows the architecture of proposed SAR RDC.
  - The SAR logic part consists of digital elements, such as D-flipflops, and has low-power characteristics. The SAR RDC consists of the preamplifier, the dynamic latch comparator, the SAR logic, and a 12-bit resistor array.
  - The preamplifier is implemented by the integrator structure using the CDS technique. The adopted CDS technique can reduce the 1/f noise and the input DC offset of the amplifier.

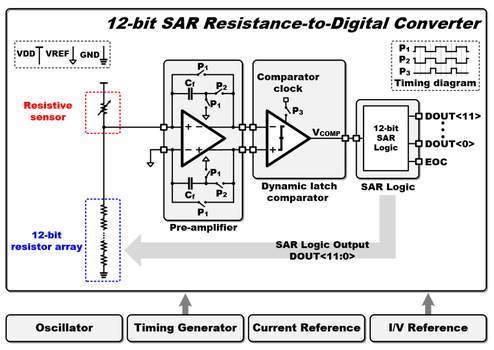

Fig. 1. Architecture of the proposed low noise chopper multipath amplifier

- Analysis of preamplifier for SAR RDC
  - The preamplifier is operated in two phases (P1 and P2). Fig. 2 shows the circuit operating at each of these two phases. The SAR RDC requires a non-overlapping clock with phases P1, P2, and P3. The proposed sensor interface IC includes a timing generator and a reference bias block.
  - The timing generator generates the non-overlapped and the SAR clocks using the 64 kHz output of the internal ring oscillator. In the P1 phase, the low-frequency noise and the DC offset of the amplifier are stored in the feedback capacitor. During the P2 phase, the preamplifier is operated as an integrator. The dynamic latch comparator operates in P3 phase.
  - The SAR logic controls the 12-bit resistor array with the comparator output. Based on the searching from the MSB to the LSB for all 12 clocks signals, the 12-bit digital code is output when the end of the clock (EOC) rises. The timing generator generates the clock needed for the SAR RDC. The clock of the SAR logic uses 16 kHz clocks and the EOC rises every 16 clocks.

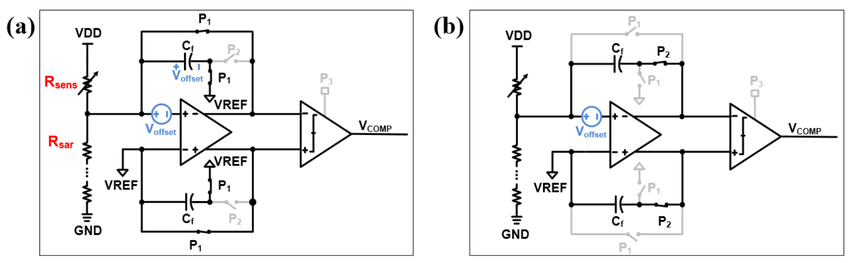

Fig. 2. Circuit operating of (a) P1 phase and (b) P2 phase

EXPERIMENTAL RESULT

- Die photograph and measurement result linearity of the fabricated SAR RDC

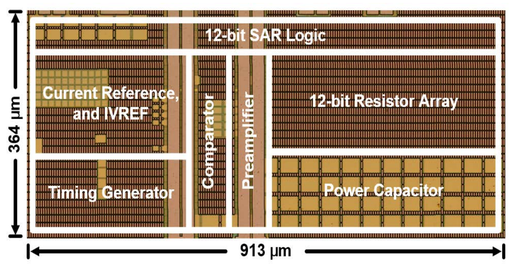

Fig. 3. Die photograph

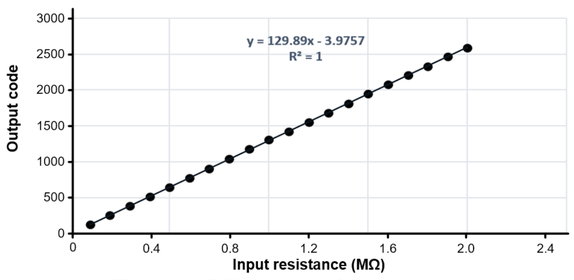

Fig. 4. Measured linearity

- Measured result of sensing the changing resistor array

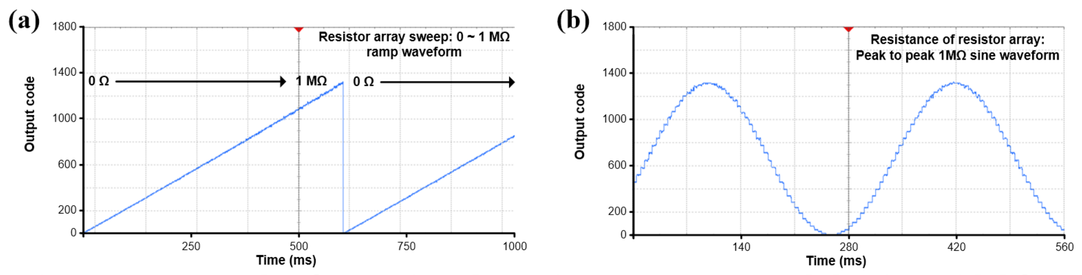

Fig. 6. Output code of sweeping the resistor (a) ramp and (b) sinusoidal form

- Output code variation and input and histogram for a fixed 1 MΩ resistor input

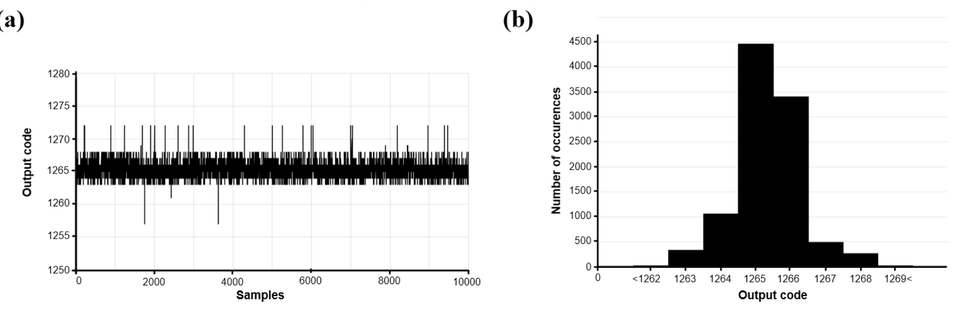

Fig. 7. Output (a) code variation and (b) histogram of 10000 samples

Table. 1. Performance comparison : summary of measured parameters

Parameter	This work	R. Wu, et al. (2012)	M. A. Ghanad , et al. (2014)	T. T. Nguyen, et al. (2014)	K. C. Koay, et al. (2017)
Process (µm)	0.18	0.7	0.18	0.09	0.065
Output signal	Digital	Digital	Digital	Digital	Digital
Supply voltage (V)	1.8	5	1.5	1	1
Power (µW)	90	1350	15	52	12.3
Input range	0-2 MΩ	± 40 mV (Bridge)	49.5-98 kΩ	± 76 Ω (Bridge)	± 9.38 mV (Bridge)
Measurement time (ms)	0.92	170	0.1818	0.096	0.5
Effective resolution (bit)	12	20	7.6	7.03	9
FoM (pJ/conversonstep)	20	218	14	38	12

CONCLUSION

- A low-power 12-bit SAR RDC for various resistive sensors is presented.
- The resistance of sensor is directly converted to a 12-bit digital output code by the comparator and the SAR algorithm.
- The dynamic latched comparator and the digital SAR logic have low-power characteristics. The proposed SAR RDC employs a preamplifier with low-noise characteristics by applying the CDS technique.
- The power consumption of the proposed SAR RDC was 93.2 µW with 1.8 V power supply. The proposed low power SAR RDC has non-linearity characteristic of 0.58% FSO, and the effective resolution was 11.3 bits within a conversion time of 0.92 ms, and an energy efficiency FoM of 33 pJ/conversion-step.

ACKNOWLEDGEMENT

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